Serial No.:	10/718,530	Art Unit:	2818

IN THE ABSTRACT

Please amend the Abstract to read as follows:

~~An integrated circuit comprised of at least one semiconductor memory array and logic circuits. The memory array includes electrically conductive word lines. The logic circuits include logic transistors with electrically conductive gates. The gates of the logic transistors and the word lines are composed of polysilicon and a metal layer. The metal layer is thicker than the polysilicon layer in the word lines; and the metal layer is thinner than the polysilicon layer in the gates of the logic transistors.~~

An integrated circuit device including at least one semiconductor memory array region and logic circuits including a support region is formed by the following steps. Form a sacrificial polysilicon layer over the array region. Form a blanket gate oxide layer over the device. Form a thick deposit of polysilicon in both the array region where word lines are located and in the support region where the logic circuits are located. Remove the thick polysilicon layer, the gate oxide layer and the sacrificial polysilicon layer only in the array region. Then deposit a thin polysilicon layer in both the array region and support regions. Next deposit a metallic conductor coating including at least an elemental metal layer portion over the thin polysilicon layer. Then form word lines and gate electrodes in the array region and support region respectively.